

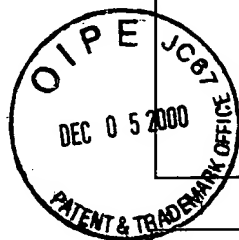
#12

PTO-1449 (Modified)  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 28, 2000	GROUP ART UNIT 2781 2181

RECEIVED

DEC 07 2000

OFFICE OF PETITIONS


 INFORMATION DISCLOSURE  
STATEMENT  
BY APPLICANT

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
Per Ver	4,633,735	05/05/87	Novak, et. al	—	—	
Per Ver	5,684,753	11/04/97	Hashimoto, et al	—	—	
Per Ver	4,322,635	03/30/80	Redwine	—	—	
Per Ver	5,006,982	04/09/91	Ebersole et al.	—	—	
Per Ver	4,636,986	01/13/87	Pinkham	—	—	

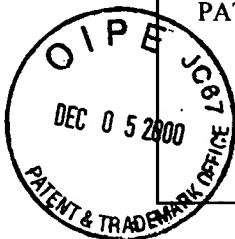
## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Per Ver	Ikeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4Md Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
Per Ver	Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985)
Per Ver	Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
Per Ver	Graham, Andy et al., "Pipelined static RAM endows cache memories with 1-ns speed", Electronic Design pp. 157-170 (Dec. 1984)
Per Ver	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," IEEE International Solid-State Circuits Conference, (Feb. 1976)
Per Ver	Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
Per Ver	Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)

EXAMINER <i>Glen Aune</i>	DATE CONSIDERED <i>1/12/2001</i>
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	



PTO-1449 (Modified)  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA001C10	SERIAL NUMBER 09/514,872
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE FEBRUARY 28, 2000	GROUP ART UNIT 2781 2181

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,979,145	12/18/90	Remington et al.	—	—	
MA	5,276,846	01/04/94	Aichelmann Jr., et. al	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DA	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)
MA	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
MA	Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)

EXAMINER Glenn Aune	DATE CONSIDERED 1/12/2001
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	